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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,713	02/19/2004	Jae-Yeong Park	0630-1970P	3186

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,713	PARK, JAE-YEONG	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-18* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 6 is objected to because of the following informalities: The word "plan" on lines 15, 17 and 21 should be "plane". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 recites the limitation "film bulk acoustic filters formed at a lower surface of the semiconductor chip" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. Claim 7 recites that the semiconductor chip comprises, in part, a "film bulk acoustic filter formed at an upper surface of a semiconductor substrate", but it makes no mention of any filter formed on the lower surface of the semiconductor chip.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes

of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ruby et al.. As to claim 1, Ruby et al., Figures 2 and 4, discloses a film bulk acoustic resonator comprising a semiconductor substrate (42), a lower electrode of two layers (112) and (113) (paragraph 0052) formed at an upper surface of the semiconductor substrate, a piezoelectric layer (114) deposited on an upper surface of the lower electrode, and an upper electrode of two layers (57) and (58) formed at an upper surface of the piezoelectric layer (54). The disclosure of Figures 2 and 4 may be combined into an embodiment which combines the bilayer top electrode and the bilayer bottom electrode.

As to claim 2, Ruby et al. discloses (paragraph 0032 and 0033) that the electrodes may be formed from molybdenum and another suitable material. Such suitable materials are recognized in the art to include titanium, chromium and tungsten (See Ella et al., bottom of paragraph 0002).

Claims 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by applicants admitted prior art. As to claim 3, applicants prior art, Figures 1C and 2, disclose a duplex filter comprising a semiconductor substrate (31), a transmission side film bulk acoustic filter (41) formed at an upper surface of the semiconductor substrate as a plurality of film bulk acoustic resonators connected serially (S) and in parallel (P), a reception side film bulk acoustic filter (42) as a plurality of film bulk acoustic resonators connected serially (S) and in parallel (P), and a plurality of passive elements (43) formed at one side of the transmission side film bulk acoustic filter and the reception side film bulk acoustic filter.

As to claim 4, applicants prior art, Figure 1C, discloses the duplexer filter further comprising an insulating film (32) between the film bulk acoustic resonator and the semiconductor substrate.

Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Bradley. Bradley, Figures 3 and 4A, discloses a semiconductor package comprising a semiconductor chip having a transmission side film bulk acoustic filter (130)(paragraph 0017) and a reception side film bulk acoustic filter (232)(paragraph 0018) formed at an upper surface of a semiconductor substrate accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel a substrate provided with a ceramic body (paragraph 0022) having a cavity of a certain space so that the semiconductor chip can be

mounted, a ground plane (408)(paragraph 0024) formed at a bottom surface of the cavity of the ceramic body, a plurality of conductive ground vias (413) connected to the ground plane for penetrating the ceramic body, and a plurality of signal wires formed from an outer circumference surface of the cavity of the ceramic body to a bottom surface thereof (412D)(412F); a plurality of conductive wires for connecting the semiconductor chip (416D)(416F), the ground plane and the signal wires; and a lid (402) for covering an upper portion of the cavity of the substrate so that the semiconductor chip and the conductive wire can be protected from the external environment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art in view of Lakin et al.. Applicants admitted prior art discloses the invention of claim 3, as described above. Applicants admitted prior art does not disclose expressly a film bulk acoustic filter for GPS at an upper surface of the semiconductor substrate. Lakin et al., in the Abstract and Figure 8, discloses a film bulk acoustic filter for GPS formed at an upper surface of a semiconductor substrate. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form a film bulk acoustic filter for GPS. The motivation for doing so would have been for use in cellular phone and other applications (Lakin et al., Summary). Therefore, it would have been obvious to combine Lakin et al. with applicants admitted prior art to obtain the invention as specified in claim 5.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bradley in view of Lakin et al.. As to claim 7, Bradley, Figures 3 and 4A, discloses a semiconductor package comprising a semiconductor chip having a transmission side film bulk acoustic filter (130)(paragraph 0017) and a reception side film bulk acoustic filter (232)(paragraph 0018) formed at an upper surface of a

semiconductor substrate accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel a substrate provided with a ceramic body (paragraph 0022) having a cavity of a certain space so that the semiconductor chip can be mounted, a ground plane (408)(paragraph 0024) formed at a bottom surface of the cavity of the ceramic body, a plurality of conductive ground vias (413) connected to the ground plane for penetrating the ceramic body, and a plurality of signal wires formed from an outer circumference surface of the cavity of the ceramic body to a bottom surface thereof (412D)(412F); a plurality of conductive wires for connecting the semiconductor chip (416D)(416F), the ground plane and the signal wires; and a lid (402) for covering an upper portion of the cavity of the substrate so that the semiconductor chip and the conductive wire can be protected from the external environment. Bradley does not disclose expressly that the semiconductor chip may be flip-chip mounted. Bradley et al., Figure 4, discloses (paragraph 0018) an FBAR filter flip-chip mounted to substrate (18). At the time of invention, it would have been obvious to a person of ordinary skill in the art to flip-chip mount the semiconductor chip within the package. The motivation for doing so would have been to reduce parasitic capacitance, consistent with known uses in the art (Bradley et al., paragraph 0005). Therefore, it would have been obvious to combine Bradley et al. with Bradley to obtain the invention as specified in claim 7.

As to claim 8, Bradley, Figure 3, discloses a plurality of passive elements (241), (243) formed on the semiconductor chip.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bradley in view of Lakin et al. and further in view of Kearns. As to claim 9, Bradley in view of Lakin et al. discloses the device of claim 7, as described above. Bradley in view of Lakin et al. does not disclose expressly that the substrate comprising LTCC or HTCC. Kearns, paragraph 0070, an FBAR which may be formed in an LTCC substrate. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form an FBAR in an LTCC substrate in the device of Bradley in view of Lakin et al.. The motivation for doing so would have been to form one of several types of filter in an LTCC substrate (Kearns, paragraph 0048). Therefore, it would have been obvious to combine Kearns with Bradley in view of Lakin to obtain the invention as specified in claim 9.

As to claim 10, Kearns, paragraph 0070, discloses that the passive elements of Bradley, which are an integral part of the filter, may be formed along with the filter within an LTCC substrate.

Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bradley in view of Bradley et al.. As to claim 13, Bradley, Figures 3 and 4A, discloses a semiconductor package comprising a semiconductor chip having a transmission side film bulk acoustic filter (130)(paragraph 0017) and a reception side film bulk acoustic filter (232)(paragraph 0018) formed at an upper surface of a semiconductor substrate accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel. Bradley does not disclose expressly that the semiconductor chip may be flip-chip mounted. Bradley et al., Figure 4, discloses (paragraph 0018) an FBAR filter flip-chip mounted to substrate (18). Bradley et al. further discloses (paragraph 0018) that the substrate (18) is ceramic, which is an insulator, that the substrate has a plurality of wiring patterns formed on an upper surface, and that the semiconductor chip is covered by a sealing layer (17) for protection from the external environment. At the time of invention, it would have been obvious to a person of ordinary skill in the art to flip-chip mount the semiconductor chip of Bradley within the package of Bradley et al.. The motivation for doing so would have been to reduce parasitic capacitance, consistent with known uses in the art (Bradley et al., paragraph 0005). Therefore, it would have been obvious to combine Bradley et al. with Bradley to obtain the invention as specified in claim 13.

As to claim 14, Bradley et al., paragraph 0018, discloses that the insulating body is ceramic.

As to claim 15, Bradley, Figure 3, discloses a plurality of passive elements (241), (243) formed on the semiconductor chip.

As to claim 16, Bradley et al., paragraph 0020, discloses an air gap (11) formed for preventing characteristics of the film bulk acoustic filters formed at a lower surface of the semiconductor chip and the passive elements formed at an upper surface of the substrate from being deteriorated between the lower surface of the semiconductor chip and the upper surface of the substrate.

As to claim 17, Bradley et al., Figure 4, discloses conductive signal paths (19) and (20) which are penetratingly formed in the insulating body (18), some of which may be grounded to ground the groundplane formed at the upper surface of the insulating body (paragraph 0021).

As to claim 18, Bradley et al., Figure 4, discloses that the plurality of wire patterns (19) and (20) formed at the upper surface of the insulating body (18) are extended outside of the semiconductor chip along the upper surface of the insulating body.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses an epoxy or polymer lid for the claimed semiconductor package. Prior art device, such as that disclosed by Bradley, use ceramic lids, such as (402) of Figure 4A (see paragraph 0024).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
September 28, 2004